

74LVC2G00

Dual 2-input NAND gate

Rev. 06 — 20 February 2008

Product data sheet

1. General description

The 74LVC2G00 provides a 2-input NAND gate function.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

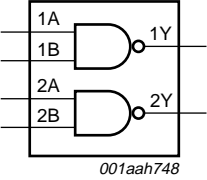
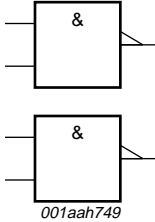
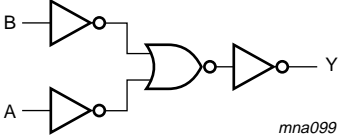
Type number	Package			Version
	Temperature range	Name	Description	
74LVC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G00GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G00GM	-40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLF based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

4. Marking

Table 2. Marking codes

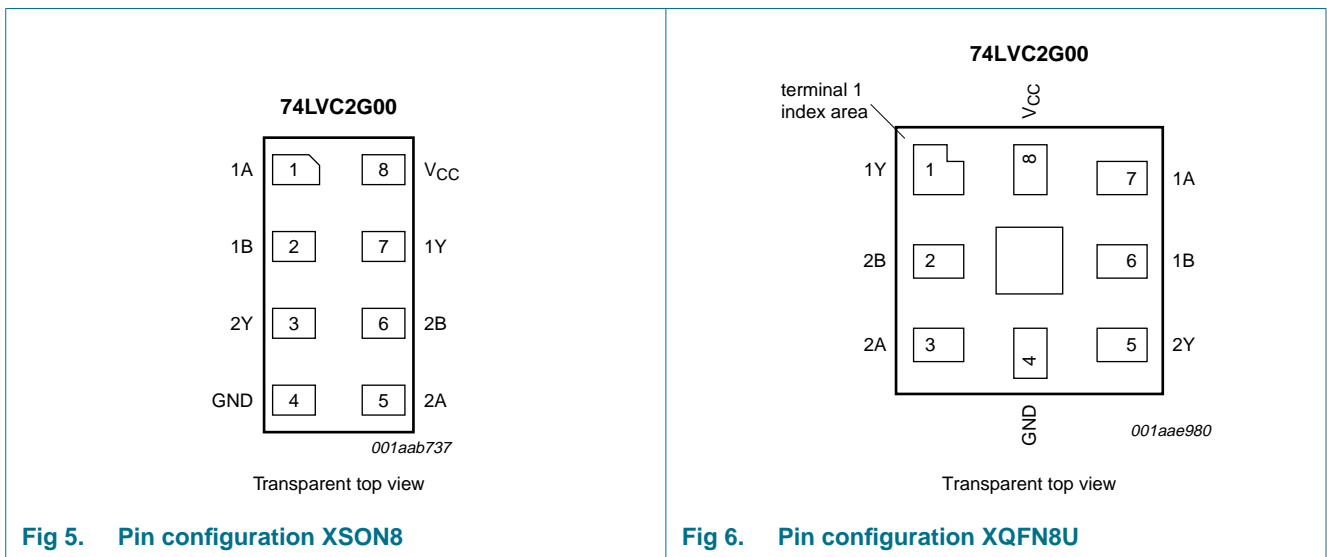
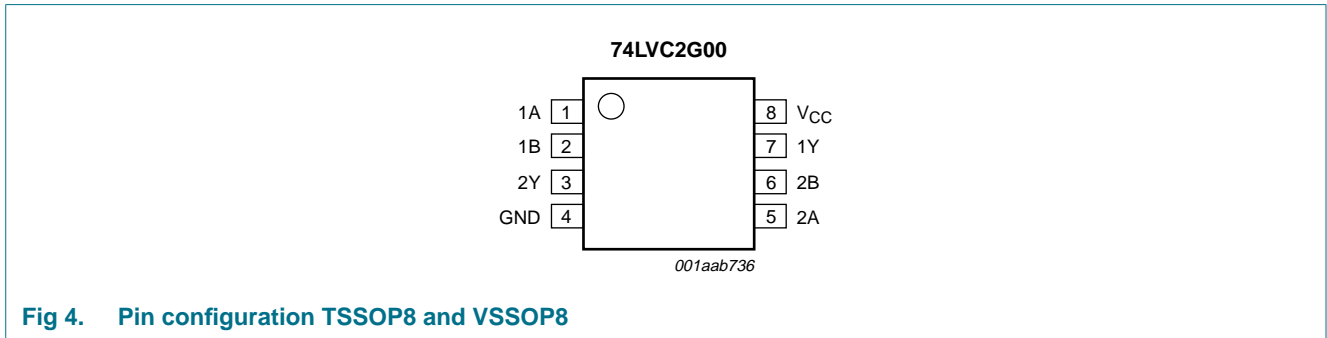
Type number	Marking code
74LVC2G00DP	V00
74LVC2G00DC	V00
74LVC2G00GT	V00
74LVC2G00GM	V00

5. Functional diagram

 <p>Fig 1. Logic symbol</p>	 <p>Fig 2. IEC logic symbol</p>	 <p>Fig 3. Logic diagram (one gate)</p>
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6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin			Description
	TSSOP8, VSSOP8	XSON8	XQFN8U	
1A	1	1	7	data input
1B	2	2	6	data input
2Y	3	3	5	data output
GND	4	4	4	ground (0 V)
2A	5	5	3	data input
2B	6	6	2	data input
1Y	7	7	1	data output
V _{CC}	8	8	8	supply voltage

7. Functional description

Table 4. Function table^[1]

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage		^[1] -0.5	+6.5	V
V_O	output voltage	Active mode	^[1] -0.5	$V_{CC} + 0.5$	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{CC}$	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.

For TXSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	1.53	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.9	2.13	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.3	2.60	-	V
		$I_O = -32\text{ mA}; V_{CC} = 4.5\text{ V}$	3.8	4.10	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$				
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	0.08	0.45	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	0.14	0.3	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	0.19	0.4	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	0.37	0.55	V
		$I_O = 32\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.43	0.55	V
I_I	input leakage current	$V_I = 5.5\text{ V or GND}; V_{CC} = 0\text{ V to }5.5\text{ V}$	-	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	$V_I\text{ or }V_O = 5.5\text{ V}; V_{CC} = 0\text{ V}$	-	± 0.1	± 10	μA

Table 7. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	0.1	10	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	5	500	μA
C_i	input capacitance		-	2.5	-	pF
$T_{amb} = -40 \text{ }^\circ\text{C}$ to $+125 \text{ }^\circ\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7 \text{ V}$ to 3.6 V	2.0	-	-	V
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65 \text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7 \text{ V}$ to 3.6 V	-	-	0.8	V
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V}$ to 5.5 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	0.95	-	-	V
		$I_O = -8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	1.7	-	-	V
		$I_O = -12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$	1.9	-	-	V
		$I_O = -24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	2.0	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100 \mu\text{A}$; $V_{CC} = 1.65 \text{ V}$ to 5.5 V	-	-	0.1	V
		$I_O = 4 \text{ mA}$; $V_{CC} = 1.65 \text{ V}$	-	-	0.70	V
		$I_O = 8 \text{ mA}$; $V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_O = 12 \text{ mA}$; $V_{CC} = 2.7 \text{ V}$	-	-	0.60	V
		$I_O = 24 \text{ mA}$; $V_{CC} = 3.0 \text{ V}$	-	-	0.80	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	± 20	μA
		V_I or $V_O = 5.5 \text{ V}$; $V_{CC} = 0 \text{ V}$	-	-	± 20	μA
		$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	-	40	μA
		$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	-	40	μA
		$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	-	40	μA
		$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 1.65 \text{ V}$ to 5.5 V ; $I_O = 0 \text{ A}$	-	-	40	μA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$; $I_O = 0 \text{ A}$; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	-	5000	μA

[1] All typical values are measured at $T_{amb} = 25 \text{ }^\circ\text{C}$.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground 0 V); for test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB to nY; see Figure 7 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.2	3.5	8.6	1.2	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	2.3	4.8	0.7	6.0	ns
		V _{CC} = 2.7 V	0.7	3.0	5.6	0.7	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	2.2	4.3	0.7	5.4	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.2	ns
C _{PD}	power dissipation capacitance	per gate; V _I = GND to V _{CC} ^[3]	-	14	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

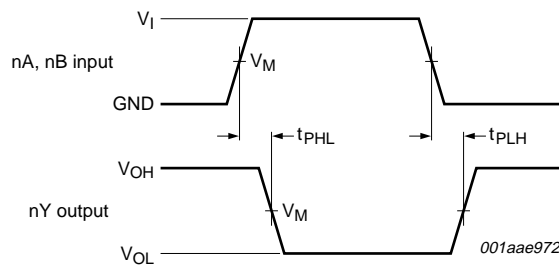
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



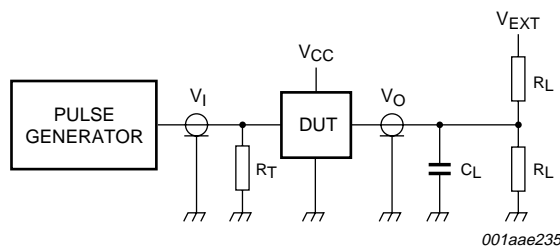
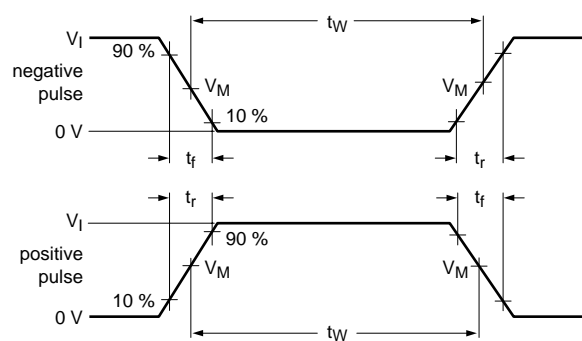
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistor

C_L = Load capacitance including jig and probe capacitance

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

V_{EXT} = Test voltage for switching times

Fig 8. Load circuitry for switching times

Table 10. Test data

Supply voltage	Input	Load	V_{EXT}
V_{CC}	V_I	C_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF, 1 k Ω , open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF, 500 Ω , open
2.7 V	2.7 V	≤ 2.5 ns	50 pF, 500 Ω , open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF, 500 Ω , open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF, 500 Ω , open

13. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

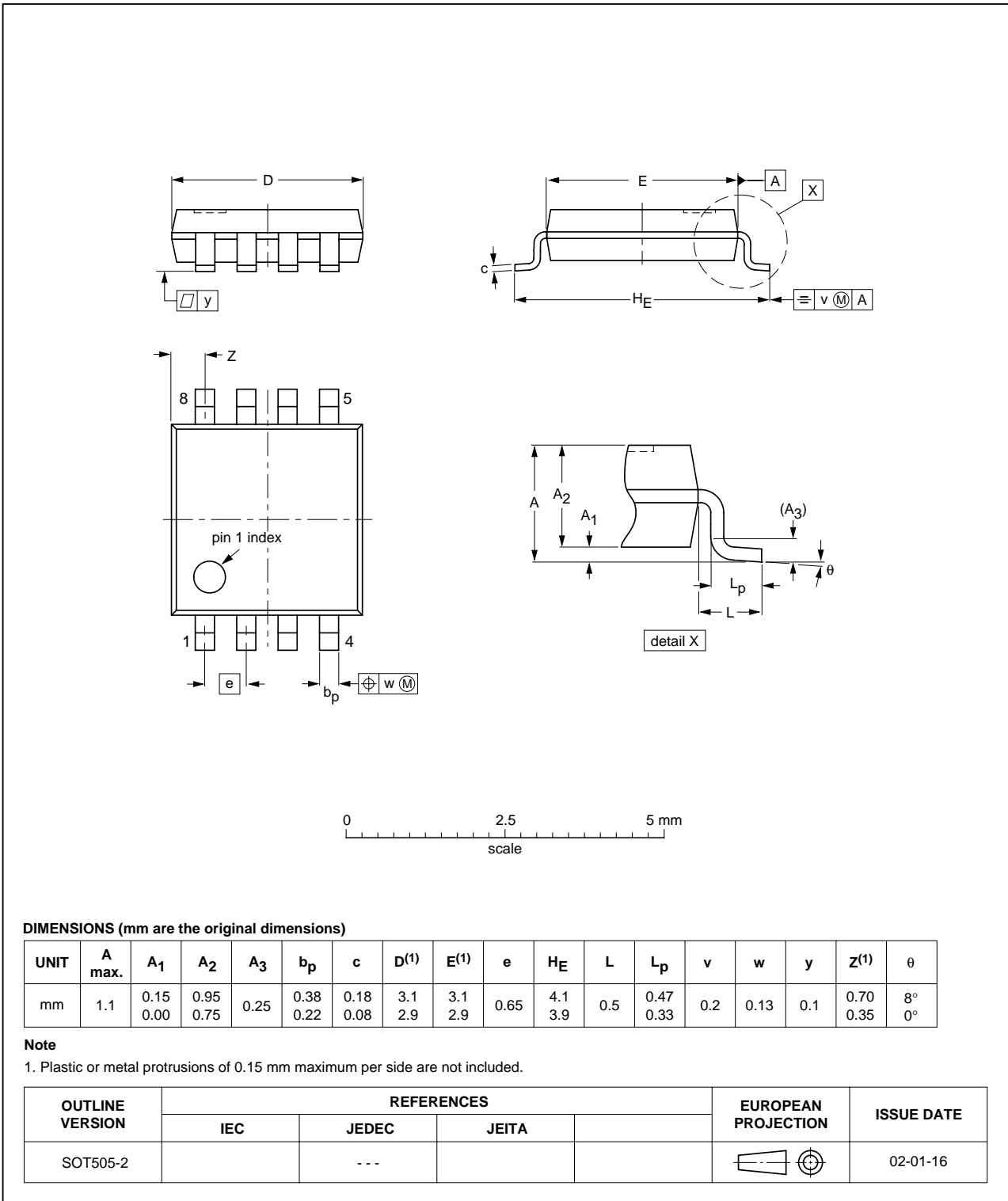


Fig 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

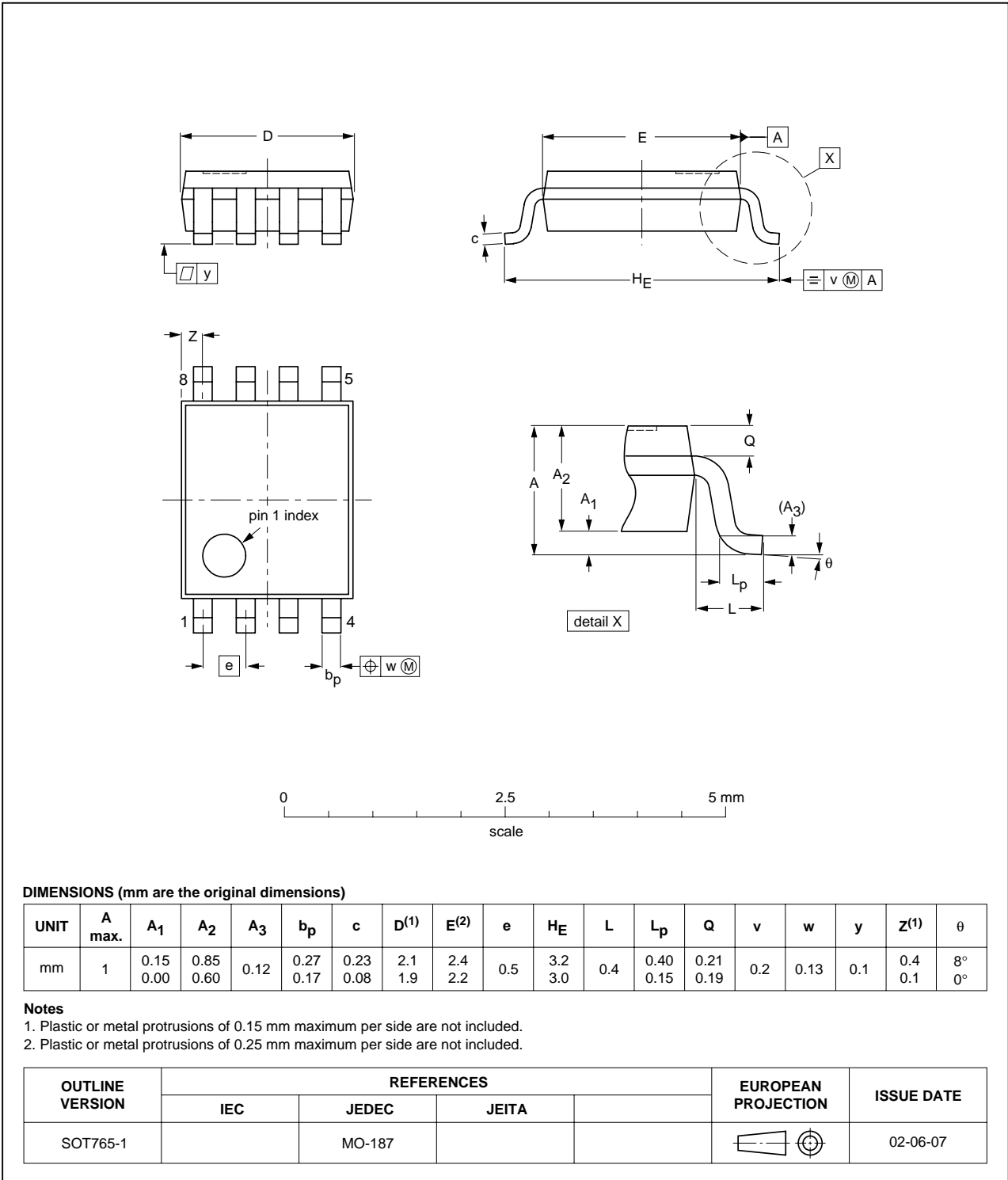


Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



Fig 11. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

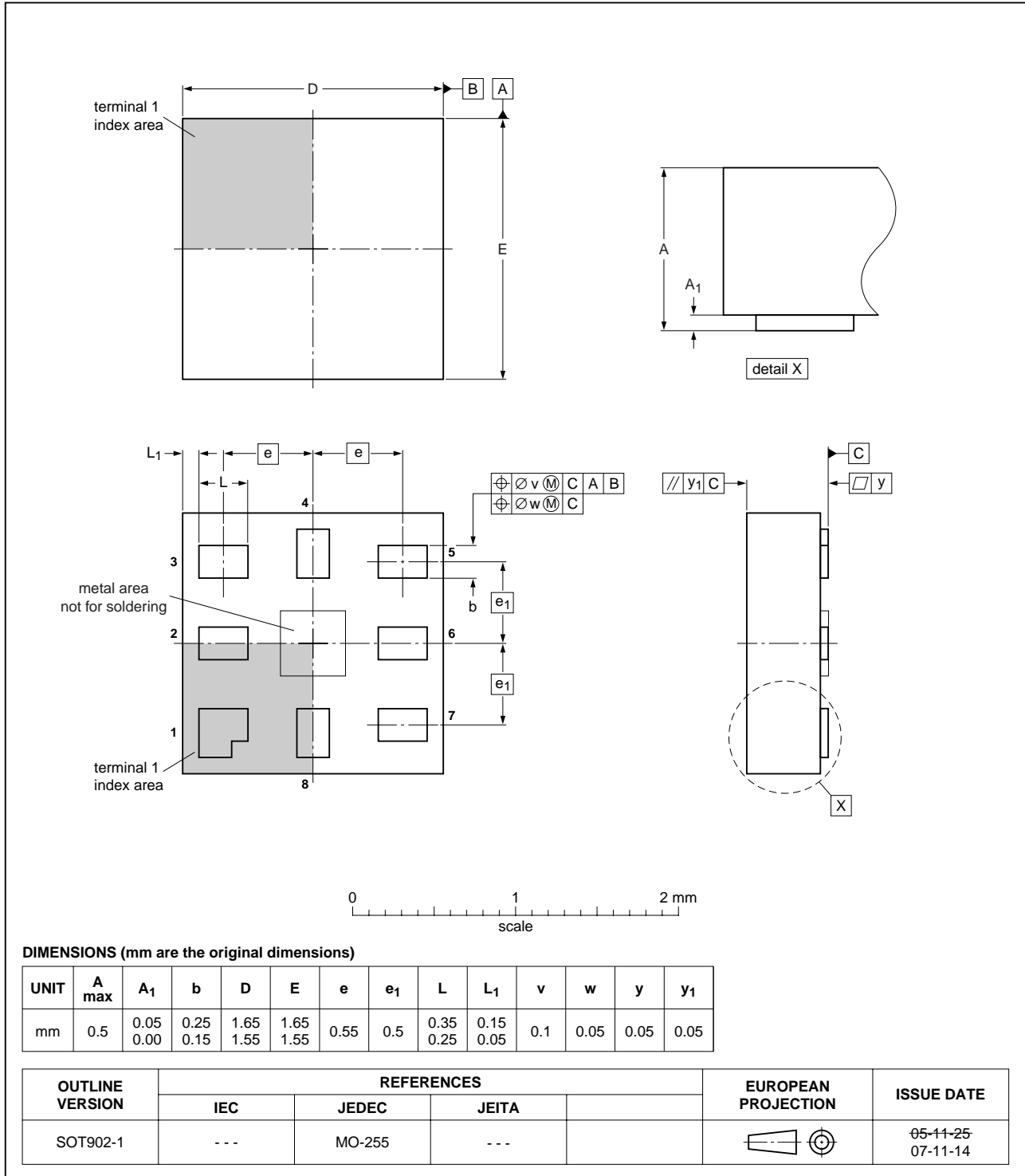


Fig 12. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G00_6	20080220	Product data sheet	-	74LVC2G00_5
Modifications:		<ul style="list-style-type: none">• Figure 1 and Figure 2: pin numbers removed• Figure 12: package outline drawing updated to latest version		
74LVC2G00_5	20070904	Product data sheet	-	74LVC2G00_4
74LVC2G00_4	20060515	Product data sheet	-	74LVC2G00_3
74LVC2G00_3	20050201	Product specification	-	74LVC2G00_2
74LVC2G00_2	20040923	Product specification	-	74LVC2G00_1
74LVC2G00_1	20031117	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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